Cat-D

EE-9/2/2021-R&D-E
Government of India
Ministry of Electronics & Information Technology
R&D in Electronics Group
(Microelectronics Development Division)

Dated: 19.05.2023

ADMINISTRATIVE APPROVAL

Subject: Administrative Approval in respect of the project entitled "Design and Development of System-on-Chip for Single-Lead Wearable Electrocardiogram (ECG) for Medical Devices" to be implemented by C-DAC Mohali, National Institute of Technical Teachers Training and Research (NITTTR) Chandigarh, University Institute of Engineering and Technology (UIET), Panjab University, Chandigarh and Sant Longowal Institute of Engineering & Technology (SLIET), Longowal under Chips to Startup (C2S) Programme.

I am directed to refer to Administrative Approval dated 18.05.2023 for the implementation of Programme "Chips to Startup (C2S) and to convey now the approval of the Competent Authority to the implementation of the above-mentioned project at a total estimated cost of Rs. 363.32 Lakh (Rupees Three Crore Sixty Three Lakh Thirty Two Thousand only) as grant-in-aid from Ministry of Electronics and Information Technology. The duration of the project is 3 Years 6 Months. The details of the project are given in the enclosed **Annexure-I**.

2. This issues with the approval of Secretary, MeitY vide computer No. 3080449 dated 03.05.2023 and concurrence of JS&FA, Ministry of Electronics & Information Technology vide computer No. 3080449 dated 03.05.2023.

Meenakshi 19/5/2023
(Meenakshi Kumar)
Under Secretary to Govt. of India

1. The Pay & Accounts Office (PAO), MeitY
2. Office of the Principal Director of Audit, Finance & Communications, Civil Lines, Near Old Secretariat, Shamnath Marg, New Delhi -110 054.
3. Prof. Balwinder Singh, Chief Investigator, CDAC, Mohali, A-34, Phase-8, Industrial Area, Sector 73, Sahibzada Ajit Singh Nagar, Punjab -160071
4. Prof. Sandeep Singh Gill, Chief Investigator, Dept. of ECE, National Institute of Technical Teachers Training and Research, Sector-26, Chandigarh-160019
5. Prof. Arvind Kumar, Chief Investigator, ECE Dept., UIET Block-II, Panjab University, Chandigarh- 160036
6. Prof. Jagpal Singh Ubhi, Chief Investigator, Dept. of ECE, Sant Longowal Institute of Engineering and Technology (SLIET), Longowal, Punjab- 148106
7. DG(NIELIT)/CFO(NIELIT)
8. GC(SV)/GC(AKP)/Sci. 'E'(NG)/Sci. 'D'(HG)/DS(DKS), MeitY
9. Finance Division/HRD/D&D Section, MetitY
10. Master Sanction file.

Annexure-I

1	**Name of the Project**	Design and Development of System-on-Chip for Single-Lead Wearable Electrocardiogram (ECG) for Medical Devices
2	**Objective & Deliverables**	**Objectives:** • To design a high input impedance(MΩ) Instrumentation Amplifier for the signal amplifications with low frequency and noise rejection for ECG. • Design and Development of a series of filters i.e., LPF, HPF and Notch filters for frequencies of design interest. • Design of 10-bit Analog to Digital Converter (ADC) for providing digital input to the microcontrollers for wireless communication. • Design and Implementation of Power efficient CMOS Low Dropout (LDO)/DC-to-DC Converter Voltage Regulator for ECG module. • Integrations & Timing closure of ECG modules (Instrumentation amplifiers, filters, ADC, and power supply unit). • Validation, Physical Simulation Signoff, and tape-out of the final ECG SoC module. • Testing/Clinical Trials/Validation of the ECG-SoC and final product delivery/ToT for commercialization. **Deliverables:** • High input impedance (MΩ) Instrumentation Amplifier IP Core • Low Pass, High Pass, and Notch filter IP Cores • 10-bit Analog to Digital Converter (ADC) IP Core • CMOS Low Dropout (LDO) Voltage Regulator or DC-to-DC Converter IP Core • Wearable ECG SoC • Skilled manpower development • FDP/Workshop/Conference • Patent/Publications • Full ecosystem knowledge generation for ECG SOC development • Circuit Schematics/Simulation models • Layout/GDSII generation of ECG analog IP cores • Design/Simulation/implementation documentation
3	**Year wise Milestones**	Annexure A
4	**Name of Implementing Agencies and Legal Status**	**Lead Agency:** C-DAC Mohali (one of the centre of Autonomous body under MeitY)

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Collaborating Agencies:

1. National Institute of Technical Teachers Training and Research (NITTTR) Chandigarh (Government Institute,
2. University Institute of Engineering and Technology (UIET), Panjab University, Chandigarh (Government Institute)
3. Sant Longowal Institute of Engineering & Technology (SLIET), Longowal (Government Institute [Deemed-to-be-University], Under Ministry of Education)

5. Total Project Duration 3 Years and 6 Months

Expected date of commencement: Date of 1st release of GIA

Expected date of completion: 3 years and 6 months from the date of 1st release of GIA or date of completion of C2S Programme (i.e. 10.02.2027), whichever is earlier

6. Total Project Outlay (GEN Budget Head): Rs. 363.32 Lakh

A. Cumulative Budget Outlay of the Project (Year wise):

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)				
	1st Year	2nd Year	3rd Year	4th Year	Total
Capital Equipment	36.00	8.00	5.00	0.00	**49.00**
Consumable Stores	9.50	9.50	8.00	8.00	**35.00**
Duty on Import	0.00	0.00	0.00	0.00	**0.00**
Manpower	55.08	55.08	59.52	29.76	**199.44**
Travel & Training	6.50	6.80	12.00	11.00	**36.30**
Contingencies	9.50	9.50	11.00	10.50	**40.50**
Overheads, if any	0.79	0.80	0.91	0.58	**3.08**
Grand Total	**117.37**	**89.68**	**96.43**	**59.84**	**363.32**

B. Agency wise Budget Outlay (Year Wise):

1. C-DAC Mohali Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)				
	1st Year	2nd Year	3rd Year	4th Year	Total
Capital Equipment	18.00	2.00	2.00	0.00	**22.00**
Consumable Stores	2.00	2.00	2.00	2.00	**8.00**
Duty on Import	0.00	0.00	0.00	0.00	**0.00**
Manpower	10.44	10.44	14.88	7.44	**43.20**
Travel & Training	2.00	2.30	3.00	2.00	**9.30**
Contingencies	2.00	2.00	2.00	1.50	**7.50**
Overheads, if any	0.16	0.17	0.22	0.13	**0.68**
Grand Total	**34.60**	**18.91**	**24.10**	**13.07**	**90.68**

2. NITTR Chandigarh Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)				
	1st Year	2nd Year	3rd Year	4th Year	Total
Capital Equipment	6.00	2.00	1.00	0.00	**9.00**
Consumable Stores	2.50	2.50	2.00	2.00	**9.00**
Duty on Import	0.00	0.00	0.00	0.00	**0.00**
Manpower	14.88	14.88	14.88	7.44	**52.08**
Travel & Training	1.50	1.50	3.00	3.00	**9.00**
Contingencies	2.50	2.50	3.00	3.00	**11.00**
Overheads, if any	0.21	0.21	0.23	0.15	**0.80**
Grand Total	**27.59**	**23.59**	**24.11**	**15.59**	**90.88**

3. UIET, Chandigarh Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)				
	1st Year	2nd Year	3rd Year	4th Year	Total
Capital Equipment	6.00	2.00	1.00	0.00	**9.00**
Consumable Stores	2.50	2.50	2.00	2.00	**9.00**
Duty on Import	0.00	0.00	0.00	0.00	**0.00**
Manpower	14.88	14.88	14.88	7.44	**52.08**
Travel & Training	1.50	1.50	3.00	3.00	**9.00**
Contingencies	2.50	2.50	3.00	3.00	**11.00**
Overheads, if any	0.21	0.21	0.23	0.15	**0.80**
Grand Total	**27.59**	**23.59**	**24.11**	**15.59**	**90.88**

4. SLIET, Longowal Budget Outlay

Budget Head	Year Wise Budget Requirement (Rs. In Lakhs)				
	1st Year	2nd Year	3rd Year	4th Year	Total
Capital Equipment	6.00	2.00	1.00	0.00	**9.00**
Consumable Stores	2.50	2.50	2.00	2.00	**9.00**
Duty on Import	0.00	0.00	0.00	0.00	**0.00**
Manpower	14.88	14.88	14.88	7.44	**52.08**
Travel & Training	1.50	1.50	3.00	3.00	**9.00**
Contingencies	2.50	2.50	3.00	3.00	**11.00**
Overheads, if any	0.21	0.21	0.23	0.15	**0.80**
Grand Total	**27.59**	**23.59**	**24.11**	**15.59**	**90.88**

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7. **Implementation Modalities** : CDAC Mohali as Lead Agency is responsible for overall implementation of the Project.

8. **Mode and extent of funding** : **As indicated below:**

(i) Budgetary Support

(a) Grants-in-aid from MeitY : Rs. 363.32 Lakh
(b) Loan : NIL

(ii) Internal generation : NIL

(iii) External Agency, if any : NIL

9. **Stages of release**

Release No.	**Pre-condition/ Stages**	**Documentation to be supplied by Implementation Agency**	**Amount to be released**
1st release	Initiation of the project	Acceptance of Terms and Conditions governing Grants-in-aid.	Rs. 34.60 Lakh (CDAC Mohali)
			Rs. 27.59 Lakh (NITTTR)
			Rs. 27.59 Lakh (UIET)
			Rs. 27.59 Lakh (SLIET)
2nd and subsequent releases	Recommendations of the PRSG & satisfactory progress report of the project	a) Submission of Utilization Certificate of the previous release. b) Technical & Financial Progress Report. **c)** Audited Statement of Accounts (at the time of Project Closure).	Rs. 56.08 Lakh (CDAC Mohali)
			Rs. 63.29 Lakh (NITTTR)
			Rs. 63.29 Lakh (UIET)
			Rs. 63.29 Lakh (SLIET)
		Total	**Rs. 363.32 Lakh**

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Year-wise deliverables/Outcomes with specific intermediate milestones

Year	Quarterly Milestones	Timelines	Outcomes	Responsible Institutions
1st	Literature survey	1st Quarter	Literature study report. Specifications. Functionality verification. Post layout netlist with parasitics for accurate prediction of functionality	C-DAC, Mohali (Nodal Centre)
	Finalize Specification	2nd Quarter		
	Designing of CMOS analog low pass filter	3rd Quarter		
	Start designing 5th ordered RC coupled filter	4th Quarter		
2nd	Finalize 5th ordered RC coupled filter design	1st Quarter	Pre Versus post-layout result validations of low pass filter. Functionality verification of analog RC coupled 5th order low pass filter. Layout of proposed analog RC coupled 5th order low pass filter Extraction for average power, leakage currents, energy consumption, and RC parasitics	C-DAC Mohali (Nodal Centre)
	Start designing CMOS analog high pass filter design	2nd Quarter		
	Finalize CMOS analog high pass filter design	3rd Quarter		
	Starting the CMOS analog Notch/Bandpass filter design	4th Quarter		
3rd	Finalize CMOS analog Notch/Bandpass filter design and unity gain buffer design	1st Quarter	Verification of functionality of high pass filter and CMOS analog Notch/Band-pass filter, Post-layout verification of high pass filter and CMOS analog Notch/Band-pass filter. Parameter extraction for average power, leakage currents, energy consumption.	C-DAC Mohali (Nodal Centre) C-DAC Mohali (Nodal Centre)
	DRC check and layout generation and Post Layout Simulations	2nd Quarter		
	Optimization for low power and compactness	3rd Quarter		
	High accuracies of the designed filters	4th Quarter		
4th	Working and Generate of GDSII files, Unity gain buffer attachment, Redesigning/optimization	1st Quarter	Verification of functionality of CMOS unity gain buffer. Pre Versus post-layout result validations of unity gain buffer. Integration & testing of designed filters in ECG SoC. Redesign/re-layout, GDSII & Documentation	C-DAC Mohali (Nodal Centre)
	Create data sheets, manuals and Reports, paper	2nd Quarter		

Year	Quarterly Milestones	Timelines	Outcomes	Responsible Institutions
1st	Detailed literature review	1st Quarter	Simulated results and verification of functionality of existing structure of Instrumentation Amplifiers. Post layout verification of Existing structure with post layout netlist.	NITTTR, Chandigarh (Participating Institute)
	Study and Design of latest existing structure of Instrumentation Amplifiers at 180nm	2nd Quarter		
	Simulation and physical design of existing structure of Instrumentation Amplifiers at 180nm	3rd Quarter		

	Selection of performance parameters and specifications	4th Quarter		
2nd	Design differential difference amplifier (DDA) using CMOS technology.	1st Quarter	Bench mark data for comparison. Verification of functionality of DDA Instrumentation Amplifiers. Design of layout of low power Instrumentation Amplifiers structure. Parameter extraction for DDA Instrumentation Amplifiers.	NITTTR, Chandigarh (Participating Institute)
	Simulation and physical design of existing structure of Instrumentation Amplifiers.	2nd Quarter		
	Design verification of Instrumentation Amplifiers for post layout design	3rd Quarter		
	Analysis and comparison of extracted data.	4th Quarter		
3rd	Modification of circuit to meet the specifications.	1st Quarter	Verification of functionality of DDA Instrumentation Amplifiers. Parameter extraction for Low Power, high gain and CMMR for modified design of amplifier.	NITTTR, Chandigarh (Participating Institute)
	Verification of modified Instrumentation Amplifiers for pre and post layout design	2nd Quarter		
	Design check for final DDA Instrumentation Amplifiers.	3rd Quarter		
	Design simulation and analysis	4th Quarter		
4th	Comparison and validation of the circuit	1st Quarter	Data based on analysis of results.	NITTTR, Chandigarh (Participating Institute)
	Testing of DDA Instrumentation Amplifiers circuit with external SOC and Analysis of testing data for validation	2nd Quarter	Data sheet preparation of DDA Instrumentation Amplifiers. Generation of testing data. GDSII.	

Year	Quarterly Milestones	Timelines	Outcomes	Responsible Institutions
1st	Literature survey	1st Quarter	Verification of functionality of existing structure of ADC. Post layout verification of Existing structure with post layout netlist.	UIET, Chandigarh (Participating Institute)
	Finalize Specification	2nd Quarter		
	Design of latest existing structure of ADC at 180nm	3rd Quarter		
	Physical design of existing structure of ADC at 180nm	4th Quarter		
2nd	Preparing the bench-mark data for power dissipation, energy consumption, leakage power dissipation, silicon area etc	1st Quarter	Bench mark data for comparison, Verification of functionality of low power ADC. Layout of low power ADC structure. Parameter extraction for power, SNR, leakage, energy consumption.	UIET, Chandigarh (Participating Institute)
	Design of proposed low power 10-bit ADC at 180nm technology	2nd Quarter		
	Physical design of existing structure of ADC at 180nm	3rd Quarter		
	Verification of ADC for post layout design (DRC, LVS, RCX)	4th Quarter		
3rd	Analysis and comparison of extracted data.	1st Quarter	Verification of functionality of low power ADC.	UIET, Chandigarh

	Modification of circuit to meet the specifications.	2nd Quarter	Verification of functionality of low power ADC. Parameter extraction for power, SNR, leakage, energy consumption. For modified design of ADC. Layout with ERC check.	(Participating Institute)
	Verification of modified ADC for pre and post layout design.	3rd Quarter		
	ERC check for final ADC circuit.	4th Quarter		
4th	Monte carlo analysis and Validation of the circuit	1st Quarter	Graphical analysis of Monte Carlo data. Preparation of final data sheet of the low-power 10-bit ADC Generation of testing data. GDSII	UIET, Chandigarh (Participating Institute)
	Testing of ADC circuit with external SOC and Analysis of testing data for validation.	2nd Quarter		

Year	Quarterly Milestones	Timelines	Outcomes	Responsible Institutions
1st	Detailed literature review	1st Quarter	Verification of functionality of existing structure of ADC Post layout verification of Existing structure with post layout netlist. Bench mark data for comparison.	SLIET, Longowal (Participating Institute)
	Design of latest existing structure of ADC at 180nm	2nd Quarter		
	Physical design of existing structure of ADC at 180nm	3rd Quarter		
	Preparing the bench-mark data for power dissipation, energy consumption, leakage power dissipation, silicon area etc.	4th Quarter		
2nd	Design of proposed low power 10-bit ADC at 180nm technology.	1st Quarter	Verification of functionality of low power ADC. Layout of low power ADC structure. Parameter extraction for power, SNR, leakage, energy consumption.	SLIET, Longowal (Participating Institute)
	Physical design of existing structure of ADC at 180nm.	2nd Quarter		
	Verification of ADC for post layout design (DRC, LVS, RCX)	3rd Quarter		
	Analysis and comparison of extracted data.	4th Quarter		
3rd	Modification of circuit to meet the specifications.	1st Quarter	Verification of functionality of low power ADC. Parameter extraction for power, SNR, leakage, energy consumption. For modified design of ADC. Layout with ERC check and Graphical analysis of Monte Carlo data.	SLIET, Longowal (Participating Institute)*
	Verification of modified ADC for pre and post layout design	2nd Quarter		
	ERC check for final ADC circuit	3rd Quarter		
	Monte carlo analysis	4th Quarter		
4th	Validation of the circuit	1st Quarter	Preparation of final data sheet of the low-power 10-bit ADC. Generation of testing data. GDSII.	SLIET, Longowal (Participating Institute)
	Testing of ADC circuit with external SOC and Analysis of testing data for validation.	2nd Quarter		

भारत सरकार
Government of India
इलेक्ट्रॉनिकी और सूचना प्रौद्योगिकी मंत्रालय
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संख्या EE-9/2/2021-R&D-E
No.....

दिनांक 26/05/2023
Date.....

Subjects: Project entitled "Design and Development of System-on-Chip for Single-Lead Wearable Electrocardiogram (ECG) for Medical Devices" being implemented by by C-DAC Mohali, National Institute of Technical Teachers Training and Research (NITTTR) Chandigarh, University Institute of Engineering and Technology (UIET), Panjab University, Chandigarh and Sant Longowal Institute of Engineering & Technology (SLIET), Longowal under Chips to Startup (C2S) Programme.

This is certified that Prof. Surinder Singh, ECE Department, Sant Longowal Institute of Engineering & Technology, Longowal, Sangrur, Punjab is Co-Chief Investigator of project entitled "Design and Development of System-on-Chip for Single-Lead Wearable Electrocardiogram (ECG) for Medical Devices" under the Category-II of Chips to Startup (C2S) Programme with project at a total estimated cost of Rs. 363.32 Lakhs for the period of 3 Years and 6 months. The monitoring and review of the Project will be carried out by MeitY as per administrative approval issued for the project on 19th May 2023.

Hemlata Gupta

Hemlata Gupta,

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To: Prof. Surinder Singh, Co-Chief Investigator, Dept. of ECE, Sant Longowal Institute of Engineering and Technology (SLIET), Longowal, Punjab- 148106

CC: Prof. Jagpal Singh Ubhi, Chief Investigator, Dept. of ECE, Sant Longowal Institute of Engineering and Technology (SLIET), Longowal, Punjab- 148106